NEW SCHEME

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Fourth Semester B.E. Degree Examination, July/August 2005
Common to BM/EC/EE/TE/ML/IT/CS/IS
Computer Organisation

Time: 3 hrs.]   [Max.Marks : 100

Note: *Answer any FIVE full questions.*
All questions carry equal marks.

1. (a) Discuss the various generations through which the computers have evolved to the present stage. Indiate the important technological features and devices that characterised each generation. **(10 Marks)**

   (b) Distinguish between unsigned and signed integers. With examples, indicate when each type of integers will be useful. **(4 Marks)**

   (c) An integer of 32 bit size is stored in memory location in the little endian fashion. Indicate using a pseudo program, how a big endian 16-bit processor could rearrange the number and store it property for its use, back in the same location. **(6 Marks)**

2. (a) Using register transfer notation, and concept of indirect addressing of memory, show how you can rearrange an ascending sorted data array to a descending sorted array in the same memory locations. Assume the array elements are of 16-bit size, and the processor system is also 16 bit size. **(10 Marks)**

   (b) Consider the following :

   i) A subroutine may required the parameters passed to it (from the main program), in a random order and more than once.

   ii) A stack is a data structure in memory, from which the data can be accessed in a lIFO order and obviously ten stack is not a suitable data structure for handling subroutine parameters.

   iii) Yet, passing subroutine parameters through stack is perhaps the commonest way of handling subroutine parameters.

   What mechanism is employed so that the parameters are made randomly accessible to the subroutine from the stack? Explain with an example.
   (10 Marks)

3. (a) Show a circuit arrangement, whereby several devices may interrupt a processor on a single interrupt request line.

   If it is required to handle the device interrupts on a fixed priority basis, indicate in detail

   i) A hardware based method

   ii) A software based method for addressing this requirement. **(10 Marks)**

   (b) Explain the hardware registers that are required in a DMA controller chip. Why is it necessary for a DMA controller to be able to interrupt the processor? Explain. **(10 Marks)**

4. (a) Explain the significant features of any ONE of the following bases :

i) PCI ii) SCSI iii) USB. **(10 Marks)**

(b) Discuss the different types of RAM's bringing out their salient features. Give some idea of their speeds and relative costs. **(10 Marks)**

5. (a) Consider a processor system with 32 bit address capability, using 64 KB of cache, arranged to operate as a 4 way set associative cache. Work out the logic which determines cache hit or miss for this system. Assume you have 20-bit comparators available for the purpose. **(10 Marks)**

(b) Describe the circuit and operation of a 4 bit carry look ahead adder. Compare the computational time, in terms of gate propagation times for a 32 bit adder using

i)   8 numbers of 4-bit carry look-ahead adders.

ii) 4 numbers of 8-bit carry look-ahead adders.

Assume no second level of look-ahead-carry generation. **(10 Marks)**

6. (a) Indicate the computational details of multiplying two 4-bit numbers 1011 and 0101 using Booth's algorithm. Verify the result obtained. **(10 Marks)**

(b) Give the basic features of the IEEE floating point number standard. **(10 Marks)**

7. (a) Give the details of the system and the control signals for executing the following functions in a processor

i) $MOV\ R_1\ to\ R_2$

ii) $LD\ M_1\ to\ R_2\ or\ ADD\ R_1\ to\ R_2$. **(10 Marks)**

(b) Give a brief out line of the sequence of actions produced by a processor to fetch and execute an unconditional branch instruction in terms of the specific control signals produced at each clock during the whole process . **(10 Marks)**

8. (a) Indicate the various steps in designing either the hardwired control for a microprocessor or microprogrammed control for a microprocessor. **(10 Marks)**

(b) Describe the salient features of a simple microcontroller that can be embedded in systems like microwave ovens. **(10 Marks)**

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